

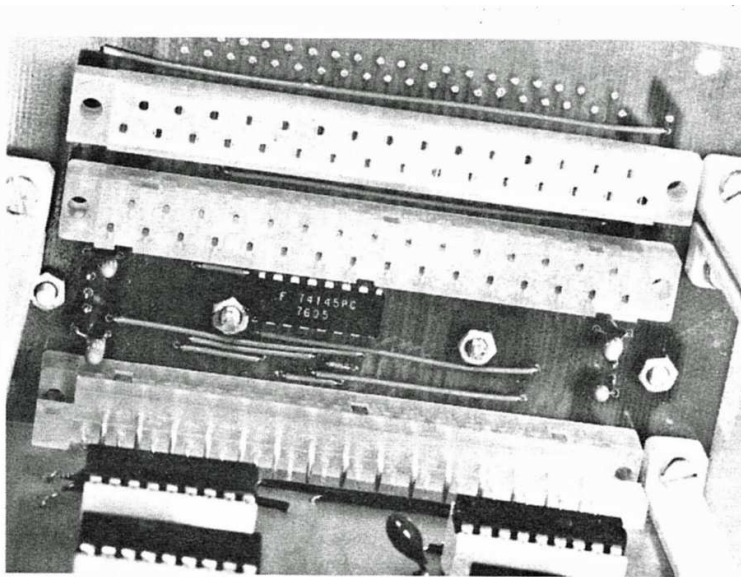


Motherboard

Memory Support for 6502 Systems

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Radio Bulletin has already described several ways to expand the standard memory of 6502 systems such as the KIM. Published so far are a 2 Kbyte static RAM card, the BEM-1 board (November 1977), a 2 Kbyte EPROM card (June and July 1978) and a 4 Kbyte static RAM card (September and October 1979). All these designs use the bus as used on the BEM-1 board, but with a number of additions, which will be needed mainly for the 4 Kbyte EPROM board in a forthcoming issue. This article describes a motherboard into which all these cards can be plugged.



It does not matter which board is placed in a connector. The connector does, however, fix the board's position in memory, because the address decoding is not done on the card itself. In addition, the buffer and decoding board described in the September 1979 issue is used. A combination of these boards and motherboards

makes it possible to expand the KIM's memory to its full size. A slightly modified version can also be used for the SYM, Junior, AIM65 and PC100, since these microcomputers broadly resemble the KIM.

Decoding

As mentioned, decoding is done in the way described in the September 1979 issue. The 64 Kbyte memory area is divided into small areas of 1 Kbyte. This is done by means of 4-to-10 decoder ICs, 74LS145, as shown in Fig. 1. Address lines A13, A14 and A15 are decoded into so-called 8KX lines. On the KIM, the "Decode Enable" line selects an

Fig. 2 shows how a number of buffer boards and motherboards are put together. From the KIM come the unbuffered address and data bus and a number of control lines. These are buffered on the first buffer board. Address lines A13, A14 and A15 are decoded into 8KX lines. The 8K1 signal, together with address lines A10, A11 and A12, is converted into select signals k8 through k15. The buffered address and data bus are passed on to the first motherboard. Lines k8 through k15 are used to select the first two connectors, each of which can hold 4 Kbytes of memory. This can be RAM,

With the 2 Kbyte static RAM card, as with the 2 Kbyte EPROM card, only signals k8 and k9 or k12 and k13 are used for selection. The 4 Kbyte RAM card uses all four select signals, i.e. k8 through k11 and k12 through k15.

Line 8K2 from the first buffer board, together with address lines A10, A11 and A12, is fed to the next motherboard and converted there into select signals k16 through k23. These lines select the last two connectors of the motherboard, which can likewise hold a maximum of 8 Kbytes of memory. Apart from 8K0, the 8KX lines have no pull-up resistor. Since the 74LS145 has open-collector outputs, this is necessary. They can be fitted on the first buffer board. A value of 470 Ω works very well. One buffer board can drive a maximum of 24 Kbytes of memory, so 32 Kbytes is too much. That is why another buffer

board must be added after a motherboard. The address and data bus are fed to it again via the preceding motherboard, as well as the 8K3 signal from the first buffer board. The decoder IC for the 8KX lines can therefore be omitted on all further buffer boards.

However, all 8KX signals used up to that point must be fed to the input of the 7400 IC on the buffer board concerned. This is to prevent cards higher up in the memory area from using the data bus at the same time when the processor performs a read. The best way to do this is to add an extra IC, the 7420, a dual NAND gate with four inputs each. How everything is to be connected is shown in Fig. 3.

Signals k24 through k31 from this buffer board are in turn fed to the next motherboard. That board carries a 74LS145 to which the 8K4 signal is applied. This produces signals k32 through k39. The procedure is repeated with the 8K5 and 8K6 signals for a buffer board and a motherboard respectively.

This makes 56 Kbytes of the total memory area addressable. The remaining 8 Kbytes can be accommodated in the last two connectors of a fourth motherboard, using its decoder IC. The 8K7 signal is applied to it. No buffer board is needed for this motherboard, because in this case exactly 24 Kbytes of memory is driven in total. Those last two connectors will usually be used for EPROMs, because the various vectors are located in this area (see September 1979 and following).

Construction

The motherboard can be built almost "with two left hands". The board layout is shown in Fig. 4 and the component layout in Fig. 5. First the wire links are fitted. Then the four tantalum capacitors and the 74LS145 IC. The board is then fitted with cheap, readily available Eurocard connectors to DIN 41617 and four card supports. A small corner is filed off one of these to make room for a bolt. The wiring between the processor, buffer board and motherboard should be kept as short as possible. Ribbon cable is best for this. Also make sure the grounding is sufficiently solid and that no ground loops have been created.

Power supply

The power supply is based on an unregulated voltage of 8 V. This comes from a transformer, for example an 8 V, 6 A type, with a bridge rectifier of, say, 10 A and a 4700 μ F smoothing capacitor. The current required depends largely on the amount of memory to be powered. A motherboard carries two regulator ICs, because four static RAM cards fitted with "low power Schottky" 2114Ls together draw about 1.7 A. Two regulator ICs (7805), each 5 V, 1 A, are therefore sufficient. A motherboard also supplies the power for a buffer board. The regulator ICs are fitted with a heat sink mounted on the back of the motherboard, see Figs. 5 and 6. The +12 V and -5 V supply voltages for a 2 Kbyte EPROM card must be fed separately to the motherboard where they are needed.

Vectors

When the 6502 is reset, a program is started whose start address is in memory locations

FFFC and FFFD (hexadecimal). On the KIM, however, addresses FFFE and FFFF coincide with 1FFE and 1FFF, because address lines A13, A14 and A15 are not decoded. When the memory is expanded they are decoded, so the KIM actually fetches its reset vector from locations FFFC and FFFD. The old situation can be restored by connecting the last 1 Kbyte select signal, k63, to the 8K0 line. When addresses FFFE and FFFF are now accessed, addresses 1FFE and 1FFF will also respond. As a result, the monitor program starts normally after a reset. If the 8K7 signal is not decoded into 1 Kbyte lines, 8K7 itself must be connected to 8K0. By connecting k63 to any 1 Kbyte signal, the reset vector can be placed at the top of any 1 Kbyte block. On the first buffer board the 8K7 line must then be disconnected from the 8K0 line.

Fig. 3 How to connect the 7420.

Fig. 4 Board layout for the motherboard, scale 1:1.

Fig. 5 Component placement, both component side and copper side.

Fig. 6 Mounting of the two voltage regulators with their heat sinks.

